# Analysis of a Switched Impedance Transformer-Type Nonsuperconducting Fault Current Limiter

Song Chen, Peng Li, Roy Ball, Jean-Francois de Palma, and Brad Lehman

***Abstract*—This paper proposes a nonsuperconducting fault current limiter (NSFCL) topology and control strategy. The switched impedance transformer-type NSFCL topology is optimized to protect against short transients and to work in conjunction with other fuses or circuit breakers, hence has the merits of being simple, low cost, and compact. A prototype has been designed and built for a three-phase 600-$V_{RMS,L-L}$ system. It has been tested in a UL-certified high-power test lab with 5-A normal current and 100-kA potential fault current.**

***Index Terms*—Bridge rectifier, fault current limiters (FCLs), high-power faults.**

## I. Introduction

With the utility grid's fast growing acceptance of distributed generators and independent power producers, the grid is continuously expanding its generating capacity to meet the increasing need for electric power. However, higher power capacity and lower source impedance, due to paralleled connection of generators, also generate larger fault currents during fault conditions [1]–[4]. The increasing fault current level may eventually exceed the maximum ratings of the existing protection devices, such as fuses, circuit breakers, and protective relays, etc. In extreme cases, large fault current surges create fire or explosion hazards by melting conductors and their insulations in the oil-filled equipment [5]. Moreover, many of the existing protective devices need several cycles to interrupt the short-circuit current. This means, in the case of a low-impedance fault, the first few high-fault current peaks pose high thermal and electromagnetic stresses on both the protection devices and any downstream equipment [6]. The natural way to solve the problem is to upgrade the conductors and the protection gear in the system. Unfortunately, this is usually expensive, complicated and in many cases, not viable given the scale of the existing power system.

In this context, an inexpensive intermediate device that is able to limit the actual fault current below the ratings of today's protection gear is desired. The purpose of this study is to introduce a new type of fault current limiter (FCL) that can help bypass or delay the costly system upgrade. As add-in devices, FCL's are subjected to the following objectives:

1) *Efficient:* the normal operating power loss should be low;
2) *Nonintrusive:* FCL should inject minimum harmonic distortion or shift of the power angle;
3) *Fast:* FCL must limit the fault current before its first peak under all fault types;
4) *Low cost:* economically beneficial—unfortunately, many FCL's do not meet this criterion, particularly if they are superconducting FCLs (SCFCLs);
5) S*mall:* Once again, FCLs normally fail to meet this criterion, due to large transformers, DC reactors, and sometimes cryogenic equipment required for operation.

For many FCLs, the fundamental philosophy is: while maintaining negligible impedance in normal operations, it must provide high impedance in the circuit during short-circuit conditions and quick transition between the normal operation and the faulted mode operation.

For several years, a number of FCL technologies have been explored and developed, many of which can provide superior technical performance [5], [7]. However, due to high cost or system complexity, the commercialization process of FCL devices has been slow. There are three major types of FCLs.

1) *SCFCL*: SCFCLs have apparent advantages in terms of normal operation power losses. But besides the high material costs, superconductors require very low-temperature environment to maintain superconducting state. Even for high-temperature superconductors, the transition temperature is typically around 100 K (−279 °F or −173 °C) [8], [9]. This means extra cost for the refrigerating equipment and power losses for the cooling.
2) *Solid-state FCL (SSFCL):* Solid-state devices are favored for their high blocking voltage and controllable characteristics [5], [10]. However, many technical issues are left to be solved before SSFCLs are widely accepted by the industry, including series–parallel stacking issues, normal state switching power losses, thermal management, control complexity and timing, reliability issues, and high cost and complexity when auxiliary circuits are needed [5].
3) *Magnetic FCL (MFCL):* MFCLs promise fast recovery and can reduce the superconducting material use since the superconducting coils works only in the dc mode. However, the devices of this type are usually bulky due to the existence of multiple low-frequency iron cores [11], [12].

To eliminate the high technology and cost barrier of the FCL types mentioned previously, various bridge-type SSFCL

Manuscript received December 5, 2013; revised May 4, 2014; accepted February 13, 2014. Date of publication July 1, 2014; date of current version November 3, 2014. Recommended for publication by Associate Editor P. Barbosa.

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Digital Object Identifier 10.1109/TPEL.2014.2329091

topologies have been proposed [13]–[19]. The principle behind an impedance inserting SSFCL, first proposed in [18] and [19], is natural and straightforward: the semiconductor switches conduct the normal operating current. Upon occurrence of fault, the switches will be blocked to force the fault current to flow on the high-impedance pass and thereby limit the current during the fault. There are many different topologies used to achieve it, but a common approach is to utilize rectifier bridges with large DC reactors [13]–[19] in which the fault current is limited by the current limiting dc reactance. With no normal-state switching and limited superconductor use, these bridge topologies provide simpler and more cost-effective FCL solutions alternative to traditional SSFCLs and SCFCLs. However, the size of elements such as large DC reactors and low-frequency transformers usually makes this type of bridge-type SSFCL bulky. In general, there are two methods to help reduce the size of the transformer. First, it is possible to create dc reactance to operate in magnetic saturation [14] when the fault occurs. Alternatively, it is possible to switch in additional resistances when the fault occurs so that the power resistor will limit the fault. In this study, we actually combine parts of both methods: When the fault occurs, we only use the small dc reactance to slow the ramp rate of the fault sufficiently so that the controller can temporarily switch in a smaller resistor. The dc reactance is permitted to slightly saturate in this short transient time. Furthermore, the power resistor is only activated for a short time until the secondary protection device clears the fault.

In some sense, NSFCLs are related to the field of dynamic voltage restorers (DVRs). There is often similarity in configuration of the bridge circuit, and the coupling transformers can be found in both devices. Both NSFCLs and DVRs can provide benefits in limiting fault currents and preventing voltage dips during fault conditions [20], [21]. Furthermore, a common feature of most DVRs, as with our FCL approach, is that the rating of the transformer required for the normal operation is much smaller than the rating required during fault. Whereas DVRs use inverters to insert the ac voltage to counteract voltage sags, the NSFCL inserts high impedance into the power line for a short transient to limit fault currents for safe operations of other protective devices.

Specifically, this study presents a new nonsuperconducting bridge-type FCL topology (NSFCL) and its specific control operation. This new NSFCL topology provides multiple benefits to the system.

1) *Low normal operation power loss:* The power losses are mainly on the small-valued resistance of the DC reactor coil and the low voltage drops on the solid-state devices (rectifier diodes and the switch).
2) *Nonintrusive:* In normal operation, the secondary winding of the transformer is short-circuited, injecting little distortion or phase shift to the main power line. Additionally, since the switching only occurs on the secondary side, the solid-state devices do not operate on the protected power line, therefore enhancing the reliability of the NSFCL. It is also safer for maintenance, since control only takes place on the secondary side.
3) *Simple but flexible control:* The control of the NSFCL is simple in that only one IGBT is used to protect all three phases. It is also flexible, providing the user with the capability to change the desired limited fault current level, so that the NSFCL can be easily coordinated with different existing protection devices.
4) *Low-fault energy let-through:* With the NSFCL, the actual fault energy allowed on the system is significantly reduced, keeping other traditional protection devices and downstream equipment from the hazards of being damaged by excessive transient fault energy.
5) *Low cost and small:* The NSFCL is specifically designed to limit the fault current for a short period of time, so that other fault interruption devices with low interrupting current ratings can safely clear the faults with high-potential fault current levels. By restraining the fault current limiting time, critical components' power stress can be substantially reduced; therefore, the size and the cost of the NSFCL can be reduced many times compared to the SCFCLs and other bridge-type FCLs in prior art. This enables the applications of the NSFCL as an intermediate add-on device to the existing protection systems and as a cost competitive alternative to expensive system upgrades.

This paper uses analytical, simulation, and experimental prototypes to analyze the operation and the performance of the NSFCL. The proposed NSFCL is introduced and operation is explained in Section II. Power losses and harmonics of the NSFCL working in both the normal mode and fault current limiting mode are evaluated in Section III. Also, best practices for sizing critical components to minimize the size and the cost of the actual implementation of the NSFCL topology are given in Section IV. Simulation results of a benchmark system to demonstrate the NSFCL's operations are shown in Sections V and VII. Finally, to validate the proposed NSFCL concept, an experimental prototype is built and tested in a UL-certified high-power lab, and the results are shown in Section VIII.

## II. Proposed NSFCL

Usually, a circuit breaker with high ampere interruption rating (AIR) and the ability to interrupt at the first zero-crossing is priced much higher than one that is slower and with low interruption rating. In this section, we show a proposed NSFCL topology that can limit the fault current level seen on the power lines, permitting the low AIR and slow circuit breakers to be used in the systems with high-potential fault current levels.

In this study, the approach in designing an FCL is fundamentally different than in most literature works [1], [5], [8], [9], [11], [12], [15], [22]–[24]. Because the actions of circuit breakers effectively limit the NSFCL's runtime in fault conditions, the NSFCL only needs to handle the high-power stresses for a short time (typically 3–5 cycles, 50–100 ms for 50/60-Hz systems). In this case, although the transient fault power is large, the total energy handled by the NSFCL is actually small. Hence, the power rating, size, and cost of the NSFCL's components can be substantially reduced.

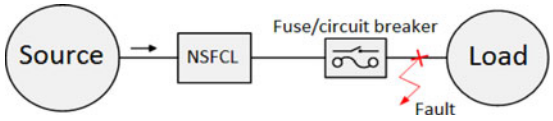


Fig. 1. Proposed FCL operates in conjunction with low AIR and slow protection devices.

Specifically, Section IV shows that the NSFCL has substantially reduced the sizes of the DC reactor and the low-frequency transformer by multiple times, compared to [15], [16], and [24]. The idea presented in this paper is a combination of new topology and control technique, along with corresponding component sizing strategies. In principle, the NSFCL is fundamentally different than other NSFCLs [15], [16], [24] in that the DC reactor is not utilized to insert high impedance into the fault current loop to limit the steady-state fault current. Instead, the DC reactor is only used to sufficiently slow down the fault transient until a very fast acting controller can switch the fault current to a high-impedance path. This separate high-impedance path is then used to clamp the fault current. We show that the size of the DC reactor will be more than ten times smaller than the state of the art.

The proposed NSFCL system operating in conjunction with low-cost fault protection devices is shown in Fig. 1. Typically, the cost of a circuit breaker with 100-kA interrupting capability would be more than twice of that with only 10-kA interruption rating, and circuit breakers with more than 200-kA AIR are rare. It is economically beneficial that the proposed NSFCL will be able to eliminate or postpone the need for ultrahigh AIR protection devices. Operating only in transients is also beneficial to the NSFCL because underrated parts (transformers, rectifier diodes, semiconductor switch, etc.) can be used, permitting the NSFCL device to shrink in size and cost substantially.

### A. Topology of the NSFCL

Fig. 2 shows the circuit configuration of the proposed three-phase NSFCL implementation. The NSFCL's topology has three major blocks.

*1) Isolation Transformers:* A set of transformers provide magnetic coupling between the main power line and the current control circuit. The primary windings of the transformers are connected in series with the main power line, and the secondary windings are wye-connected. With this configuration, the normal operation current flowing on the primary windings can be reflected to the dc side of the NSFCL and be monitored by the control circuit; whereas during fault condition, the high impedance on the current control circuit can be inserted to the primary side of the transformers. In order to demonstrate the idea of the NSFCL topology and control strategy, in this paper, 1:1 turns-ratio transformers are selected for the benchmark system. This is because our benchmark system is demonstrated for 600 $V_{AC}$ bus, which is typical of North American industrial power distribution, e.g., Canada is 600 $V_{AC}$ and the US is more toward the 480 $V_{AC}$. This permits relatively low-voltage IGBT switches to be used along with the 1:1 turns ratio for this

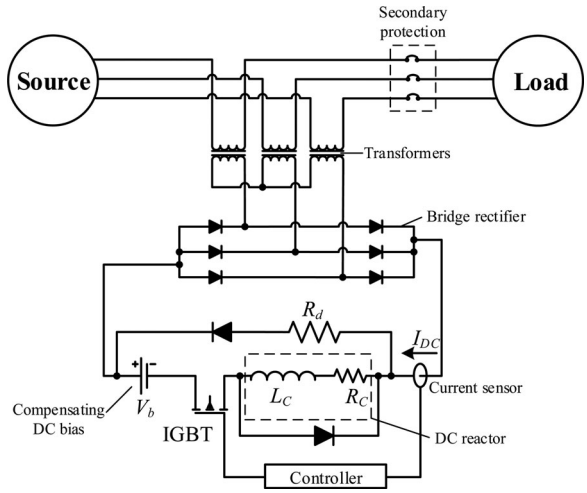


Fig. 2. Topology of the proposed NSFCL implementation. The secondary protection device is, also, often placed upstream from the transformers instead of downstream as shown. When this occurs, the secondary protection provides additional protection to the FCL.

specific, important application. Nonetheless, the turns-ratio of the transformers can be varied to adapt different system needs. For example, for medium-voltage applications, the turns-ratio $N_1 : N_2$ is preferably higher than 1, so that the voltage can be stepped down at the secondary and the dc link to possibly minimize series stacks of IGBTs, and that a smaller resistance can be used. However, in this case, the normal operating and fault currents on the secondary side will be high, posing stresses on the secondary side components. Therefore, the transformer turns-ratio should be carefully designed to achieve maximum system safety and minimum costs. Of course, as higher voltage IGBTs or IEGTs with advanced materials are developed, the permissible stress on the secondary side switches may be increased in the future. This though would likely lead to future research problems, such as proper design of the electrical insulation level and thermal management of the isolation transformer and the reactor.

*2) Bridge Rectifier:* A three-phase diode bridge rectifier converts the ac current from the transformer to the dc current for current sensing and control. This way, currents on all three phases can be monitored by one single current sensor and can be controlled by one single unidirectional semiconductor switch.

*3) Controlled Current Paths:* The dc current, continuously monitored by a current sensor, follows one of the two current paths, depending on whether in normal or faulted operation mode:

*a) Current Path (i)—normal State:* Current Path (i) is the low-impedance current path for the normal operating current, as shown in Fig. 3(a). It consists of a DC reactor ($L_c$ and $I_{\mathrm{Threshold}}$), an ON-state semiconductor switch, and a dc voltage source providing the bias voltage to compensate for the forward voltage drops on the semiconductor devices and the dc reactor's resistance. When the normal current flows on this current path, the impedance seen from the primary side of the transformer is small. In this study, a small battery is used as

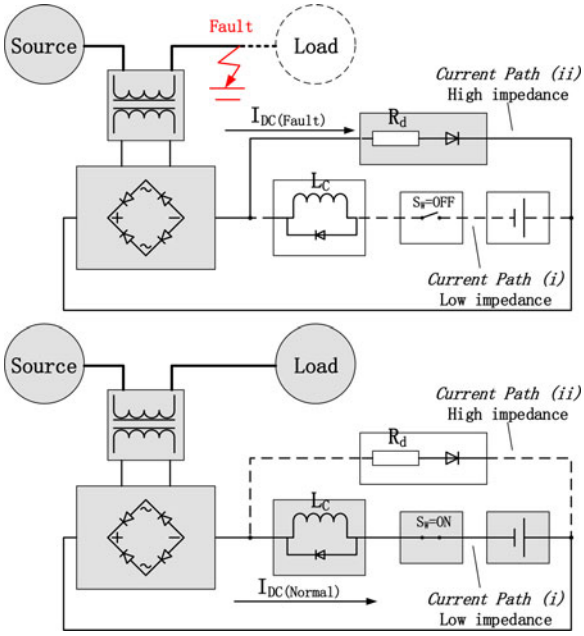


Fig. 3. Operation modes of the NSFCL: normal current on Current Path (i) and fault current on Current Path (ii).

the dc voltage source. However, commercialized NSFCL may incorporate an ac/dc converter or a dc/dc converter coupled to the transformer/rectifier.

*b) Current Path (ii)—fault state:* Current Path (ii) is the high-impedance current path that carries and limits the fault current during fault states, as shown in Fig. 3(b). It consists of a current-limiting power resistor ($R_d$). In the fault state, the semiconductor switch on Current Path (i) will be turned OFF, forcing the fault current to flow on Current Path (ii). In this case, fault energy is dissipated on the current limiting resistor; and the fault current can be limited.

### B. Operation of the NSFCL

Fig. 4 demonstrates the operation sequence of the NSFCL. During normal operation, when the current is below a preset threshold $I_{\mathrm{Threshold}}$, the IGBT is in continuous ON state. The dc branch current $I_{\mathrm{DC}}$ flows on the low-impedance Current Path (i). The dc bias voltage source $V_b$ compensates to the voltage drops on the rectifier diodes, the IGBT and the DC reactor, creating an approximate short circuit ($V_{\mathrm{Sec}} \approx 0$) across the secondary winding of the transformer. Therefore, the impedance seen at the primary winding is negligible.

When there is a fault occurring downstream, the dc current level will follow the rise of the fault current on the primary power lines. When it reaches the threshold current $I_{\mathrm{Threshold}}$, the IGBT is turned OFF to divert the current to the high-impedance path [Current Path (ii)] that consists of a resistor $R_d$ (as shown in Fig. 2). The resistance $R_d$is then reflected to the transformer primarily by the transformers and limits the fault current.

This configuration can substantially reduce the size and ratings of the NSFCL's components, in that:

1) Only the normal operating current is to flow through the components on the low-impedance path, preventing the continuous large current seen by the dc source and DC reactor. The components in the low-impedance path require low-current ratings because they only carry the normal operating current at the steady state.
2) The inserted impedance is the current limiting resistor $R_d$. The DC reactor only serves to slow down the rise of the fault current. This helps the NSFCL topology to reduce the size and the weight of the DC reactor, compared to state of the art [15], [16]. For example, in our NSFCL prototype, a 1-mH, 6-A rated inductor bank is used instead of the 100-mH, 45-A-rated reactor in [16]. This reduces the weight from 72 to 0.8 lbs. on just the DC reactor element [25]. The sizing procedure of the DC reactor will be explained and calculated in Section VI. It should be noted that with the faster controller and the semiconductor switch, the DC reactor might be further minimized or even removed from the circuitry.

## III. Operation of the NSFCL

### A. Normal Operation Mode

As an intermediate device, the NSFCL is required to be "invisible" to the system when there is no fault. In other words, in the normal operation mode, the NSFCL should have minimum power loss and inject minimum harmonic distortion to the system line current and voltage. In this section, power losses and harmonic distortion are analyzed for the NSFCL. Also, effects of critical component values are given.

Fig. 5 shows the per-phase equivalent circuit for the NSFCL in the normal operation mode. A simple nonideal transformer model is used in Fig. 5 (in dashed frame), in which the magnetizing inductance $L_M$ and winding resistances ($R_{S1}$ and $R'_{S2} = \frac{N_1^2 R_{S2}}{N_2^2}$) are modeled.

The total power loss of the NSFCL is the combination of two major parts, as follows:

$$P_{\mathrm{Total}} = V_{\mathrm{Pri}} I_{\mathrm{Pri}} + V_{\mathrm{DC}} I_{\mathrm{DC}} \tag{1}$$

where $V_{\mathrm{Pri}} I_{\mathrm{Line}}$ represents the loss seen from the power line; and $V_{\mathrm{DC}} I_{\mathrm{DC}}$ represents the power needed for the dc voltage source for bias compensation.

Fig. 6 shows the circuit diagram of the NSFCL in the normal operation, during which the dc branch current $I_{\mathrm{DC}}$ flows on the low-impedance Current Path (ii). When choosing an appropriate value for the dc bias compensation voltage ($V_{\mathrm{DC}}$), we can offset the voltage drops on the semiconductor devices and effectively short-circuit the secondary windings of the transformers. In this case, the line-to-line voltages $v_{\mathrm{ab}}$, $v_{\mathrm{ac}}$, and $v_{\mathrm{bc}}$ in Fig. 6 will be zero.

On the dc current loop shown in Fig. 6, there are two diodes and an IGBT conducting current. Therefore, according to KVL, in order to have $v_{\mathrm{ab}} = v_{\mathrm{ac}} = v_{\mathrm{bc}} = 0$, the minimum value required for $V_{\mathrm{DC}}$ is

$$V_{\mathrm{DC}} \geq \sqrt{2} I_N R_C + 2V_D + V_{\mathrm{igbt}} = \sqrt{2} I_N R_C + V_{\mathrm{SS}} \tag{2}$$

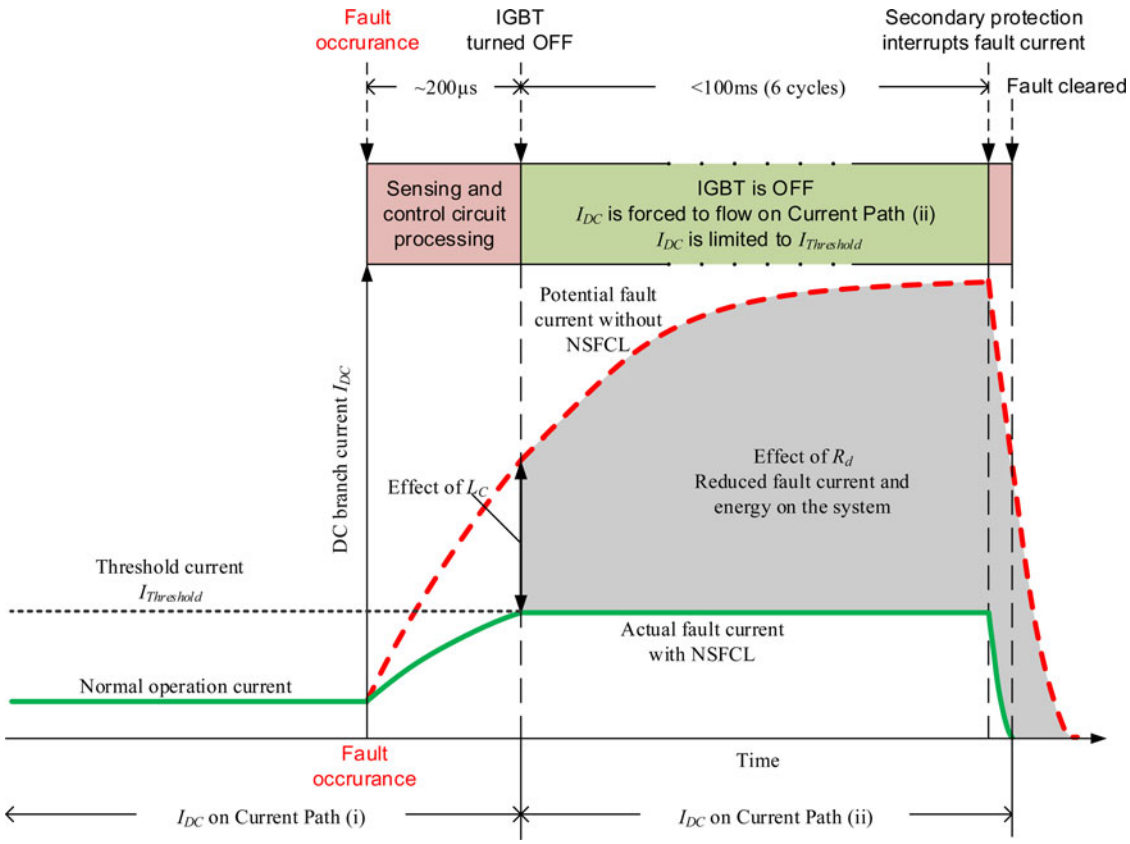


Fig. 4. Operation sequence of the NSFCL protection system.

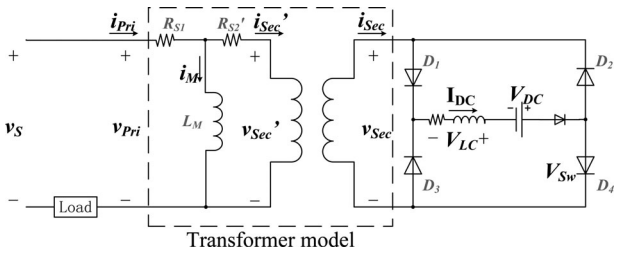


Fig. 5. Per-phase equivalent circuit under the normal operation mode.

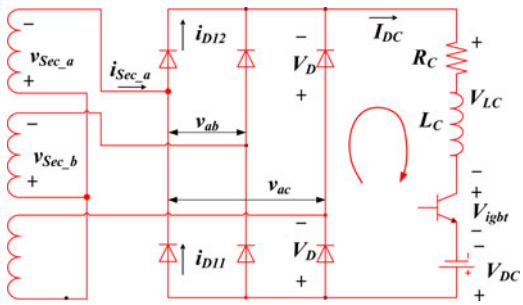


Fig. 6. NSFCL conducting circuit under the normal operation mode.

where $I_N$ is the RMS normal operation current on the power lines, $R_C$ is the resistance of the DC reactor, $V_D$ is the diode forward bias voltage, $V_{\rm igbt}$ is the IGBT's forward bias voltage, and $V_{\rm SS} = 2V_D + V_{\rm igbt}$ is the combined voltage drop on semiconductor devices. When in conduction, both $V_D$ and $V_{\rm igbt}$ can be considered to be part-dependent constant values.

When the secondary winding is shorted, $v_{\rm Sec} = 0$. Then, the primary winding voltage drop $v_{\rm Pri}$ in Fig. 5 is given by

$$\begin{aligned} v_{\rm Pri} &= i_{\rm Pri}R_{S1} + i'_{\rm Sec}R'_{S2} \\ P_{\rm loss} &= v_{\rm Pri}i_{\rm Pri} + V_{\rm DC}I_{\rm DC} \end{aligned} \tag{3}$$

where $i'_{\rm Sec}$ and $R'_{S2}$ are the transformer's secondary side parameters reflected to the primary side. Since the transformer winding resistance is normally very low, the voltage drop on the winding will be very small. The total power loss $P_{\rm loss}$ of the NSFCL has two components: 1) the power losses seen by the system due to the voltage drops across the transformer primary windings and 2) the power required by the compensating dc source, which may be also extracted from the power line or from a separate source.

### *B. Fault Current Limiting Mode*

When a fault occurs, and the line current exceeds the preset threshold current $I_{\rm Threshold}$, the semiconductor switch $S_W$ is turned OFF. The dc current is then diverted to the high-impedance path [Current Path (ii) in Fig. 3] that consists of a resistive bypass $R_d$. In this case, the NSFCL is working in the bridge rectifier mode with a resistive load $R_d$. Therefore, the maximum value of the dc current during fault is determined by

the value of $R_d$

$$i_{\mathrm{AC,max}} = I_{\mathrm{DC,max}} = \frac{v_{L-L,\mathrm{peak}}}{R_d}. \tag{4}$$

## IV. Sizing of Critical Components

The NSFCL is an intermediate device added to the system. It is important that the implementation of this topology can be made as small and low cost as possible. In this section, the sizing of critical power handling elements is discussed.

### A. Sizing Current Limiting Resistor $R_d$

From an energy point of view, the fault energy is transferred by the transformers to the dc branch of the NSFCL and is dissipated by the power resistor $R_d$. Hence, $R_d$ is a critical part to size and choose for practical applications.

*1) Determining the Resistance of* $R_{\mathrm{d}}$*:* As discussed previously, the resistance of $R_d$ determines the fault current level that is maintained by the NSFCL. Fig. 16 shows that the peak value of the line current is the same as that of the dc current $I_{\mathrm{DC}}$. Therefore, one can control the fault current level by controlling $I_{\mathrm{DC}}$. That is, $R_d$ can be determined from (10)

$$R_d \approx \frac{v_{L-L,\mathrm{peak}}}{I_{\mathrm{DC,max}}}. \tag{5}$$

This value is under the assumption of ideal transformers, and is the minimum value of $R_d$ if the desired maximum acceptable fault current level $I_{\mathrm{DC}}$ is given.

*2) Determining the Power Rating of* $R_{\mathrm{d}}$*:* In the fault current limiting mode, the power resistor $R_d$ needs to dissipate the majority of fault energy. To make sure that the resistor can survive such energy, we need to determine the power rating of the resistor.

During the fault current limiting mode, the power stress on the resistor $R_d$ is

$$P_{R_d} = I_{\mathrm{DC}}^2 R_d \tag{6}$$

which is very high and is not practical in actual implementation. However, the goal of the NSFCL is to limit the fault current only for several cycles so that the slower circuit breaker will clear the fault. Therefore, it is possible to use a resistor that has much lower power rating. This is because the power rating of resistors is based on their capability to sustain the thermal energy they generate when carrying the current. In most cases, resistor manufacturers specify the pulse power rating (or short time overloading allowance) for their products, in the form of [26]

$$P_{\mathrm{pulse,ref}} = M \times P_{\mathrm{nominal}} = \frac{P_{R_d} \times T_{\mathrm{pulse}}}{T_{\mathrm{pulse,ref}}} \tag{7}$$

where $P_{\mathrm{pulse,ref}}$ and $T_{\mathrm{pulse,ref}}$ refer to the reference pulse overload power and duration, respectively, and $P_{\mathrm{pulse,ref}}$ is in the form of $M$ times the nominal power rating. These two parameters are specified by the manufacturer. Additionally, $T_{\mathrm{pulse}}$ is the expected duration of the overload in the actual circuit and $P_{R_d}$ is the overloading power as given in (11).

A typical example of such pulse power rating can be found on the datasheet of the Vishay RH series wire-wound power resistor: five times rated power for 5 s [27]. In this case, the resistor is rated for the overload power five times of its nominal power if the overloading lasts 5 s ($M = 5$ and $T_{\mathrm{pulse,ref}} = 5\mathrm{s}$). Then, from (12), we can solve for the minimum power rating requirement for the resistor $R_d$

$$P_{\mathrm{nominal}} = \frac{P_{R_d} \times T_{\mathrm{pulse}}}{M \times T_{\mathrm{pulse,ref}}}. \tag{8}$$

With $P_{R_d}$ calculated from (11), and $T_{\mathrm{pulse}}$ chosen to be 100 ms (six cycles), the nominal power rating required for the resistor is only a fraction (0.4%) of the steady-state power rating in (11). Equation (13) indicates that, with timely actions of other fault interruption devices (six cycles after fault), the power rating of the current limiting resistor can be substantially reduced in the NSFCL.

### B. Sizing DC Reactor $L_C$

As introduced in Section III, the DC reactor used in the NSFCL is much smaller than in prior art [23]. This is achieved by reducing the required inductance ($L_C$) as well as the current rating of the DC reactor.

The purpose of $L_C$ is to increase the time constant of the system, therefore slowing down the increase rate of the fault current for electronics of the NSFCL (sensor, controller, and semiconductor switch). The sensing and control delay $\tau_E$ is defined as the time delay between when the fault current level reaches protection threshold and the IGBT is completely turned OFF. $\tau_E$ is a combined time of different delays on the sensing and control circuit

$$\tau_E = \tau_{\mathrm{Sensing}} + \tau_{\mathrm{control}} + \tau_{\mathrm{OFF,igbt}} \tag{9}$$

where $\tau_{\mathrm{Sensing}}$ is the delay of the current sensor, $\tau_{\mathrm{control}}$ is the time needed for the control circuit to make decision, and $\tau_{\mathrm{OFF,IGBT}}$ is the turn-off time of the IGBT. The inductance of the DC reactor should be sufficient to suppress the rise of the dc current so that $I_{\mathrm{DC}}$ does not exceed the maximum acceptable level $I_{\max}$ after delay $\tau_E$. Therefore, the minimum dc inductance required would be

$$L_C \geq \frac{v_{L-L,\max}}{\frac{\mathrm{d}i_{\mathrm{DC}}}{\mathrm{d}t}} \approx \frac{v_{L-L,\max}\tau_E}{I_{\max}} \tag{10}$$

where $v_{L-L,\max}$ is the magnitude of system line-to-line voltage and $\frac{\mathrm{d}i_{\mathrm{DC}}}{\mathrm{d}t}$ can be approximated by $\frac{I_{\max}}{\tau_E}$.

In the NSFCL, the DC reactor carries current only in the normal operating mode or when transitioning from the normal mode to the fault current limiting mode. The DC reactor is on the low-impedance path, which is an open circuit when the NSFCL is in the current limiting mode. The energy stored in the reactance is discharged through the antiparallel freewheeling diode (see Fig. 2). Additionally, since the transient between two operating modes is small, we only need to consider $L_C$ 's power stress during normal operation. This is typical, for instance, of when fault designs are for short time durations, such as in DVR's [20], [21]. However, it implies that it is possible to extend the approaches presented in this paper to, perhaps, modify other

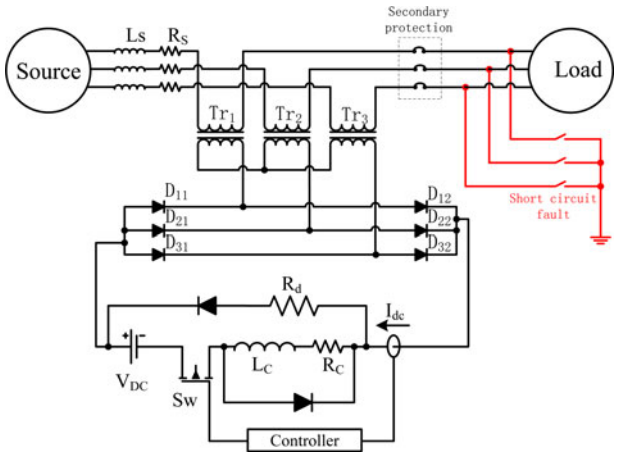


Fig. 7. Benchmark system setup.

TABLE I
PARAMETERS IN THE BENCHMARK SYSTEM

| | |
|---|---|
| **System voltage** ($V_{S,L-L}$) | $600\,\mathrm{V_{L-L}}$ |
| **Normal current** ($I_N$) | 5 A |
| **Protection threshold** ($I_{\mathrm{Threshold}}$) | 45 A |
| **Maximum limited fault current** ($I_{\mathrm{max}}$) | 50 A |
| **Potential fault current** ($I_{F,\mathrm{potential}}$) | 100 kA |
| **DC voltage source** ($V_{\mathrm{DC}}$) | 6.5 V |
| **High-impedance path resistance** ($R_d$) | 18 Ω |
| **DC reactor inductance** ($L_C$) | 1 mH |
| **Transformer turns-ratio** ($N_1 : N_2$) | 100:100 |
| **Transformer core cross-sectional area** ($\mathbf{A_c}$) | $25\mathrm{cm}^2$ |

NSFCL or SSFCL approaches [13]–[20] to operate with smaller reactors or transformers when secondary protection devices are concurrently used.

## V. Benchmark System

In this paper, a benchmark system has been designed, simulated, and experimentally tested. The three-phase benchmark system is operating with a 600-V line-to-line voltage and a balanced 5-A phase current during normal state. Short-circuit faults are created on the power lines, generating up to 100 kA of the potential fault current if the NSFCL was not used. In the experimental tests, a three-phase circuit breaker with 10-kA AIR is used as the secondary protection device. Fig. 7 shows the benchmark system configuration, and its parameters are listed in Table I. As previously noted in Fig. 2, the secondary protection is often desired to be upstream the transformer and not as shown. However, in the experimental benchmark system implemented in a UL-certified laboratory, it was required that the FCL be placed closer to the load. In fact, this provided additional safety and protection to the circuit breaker, which turned out to be far more costly than the FCL being tested.

In the benchmark system, the threshold current of the NSFCL is specified at 45 A, and the fault current is limited to 50-A peak. The NSFCL is rated for fault state operation time of 100 ms (six cycles), while the circuit breaker is able to clear the fault after one cycle.

The inductance of the DC reactor ($L_C = 1$ mH) and the high-impedance path resistance ($R_d = 18\ \Omega$) are determined using (10) and (15), according to the system parameters and the limited fault current level.

## VI. Simulation Results

In this section, results from simulations in Orcad/PSpice environment are shown to demonstrate the NSFCL's operation. Also, to show the flux status within the transformer cores, simulations using finite-element analysis software (ANSYS Maxwell 2D) are also shown. The simulation parameters are as listed in Table I.

### A. Normal Operation Mode

Fig. 8 shows the magnetic flux density in the three transformer cores under normal conditions. Since the secondary windings are effectively short circuited, there is almost no magnetic flux induced inside the cores. Therefore, the core losses during the normal operation mode should not be a concern in the transformer design for the NSFCL.

Fig. 9 shows the simulation waveform of the ac voltages under normal conditions. Only data of phase A are shown, which are sufficient for the demonstration of the balanced three-phase benchmark system. In the normal state, the secondary winding voltage $v_{\mathrm{sec}\_A}$ is nearly zero, due to the compensation of the dc bias. This means that the secondary side of the transformer has minimal effect on the primary-side operation. Due to the small resistance of the primary winding, only a small voltage drop of approximately 1 V is observed, as predicted by (4).

Fig. 10 shows the simulation waveforms of the normal operating currents. The upper plot shows the currents on the secondary side of the transformers, and the lower plot shows the ac current on the primary side. For ac currents, secondary and primary winding currents are shown for phase A. During normal operation, both diodes in a pair ($D_{11}$ and $D_{12}$ for example) are conducting all the time. The sum of the currents on these diodes equals the current in the secondary winding of the transformer.

Figs. 9 and 10 imply that the dc side of the NSFCL has little effect on the power line current during normal operation. The power lines only see the small winding resistance of the transformers' primary windings. Therefore, the power loss seen by the system would be, according to (3), the sum of each phases power loss plus the loss from the dc source. From Fig. 9, the loss per phase is 5 A × 1 V. Fig. 10 shows the secondary dc current to be $I_{\mathrm{DC}} = 8$ A. Therefore, the total power loss for the benchmark circuit is estimated as $P_{\mathrm{loss}} \sim 3 * 5\ \mathrm{W} + 8\ \mathrm{A}(6.5\,\mathrm{V}) = 67\,\mathrm{W}$ in the benchmark 5.7-kW system. A clear drawback of the approach compared to SCFCL approaches is that without superconducting materials, there is additional power loss.

### B. Fault Current Limiting Mode (Symmetrical Fault)

A symmetrical three-phase ground fault is illustrated in Fig. 11. When this fault occurs, $R_d$ is switched in and system voltages are applied to the transformer windings. Fig. 12 shows the magnetic flux density inside the cores during this operation

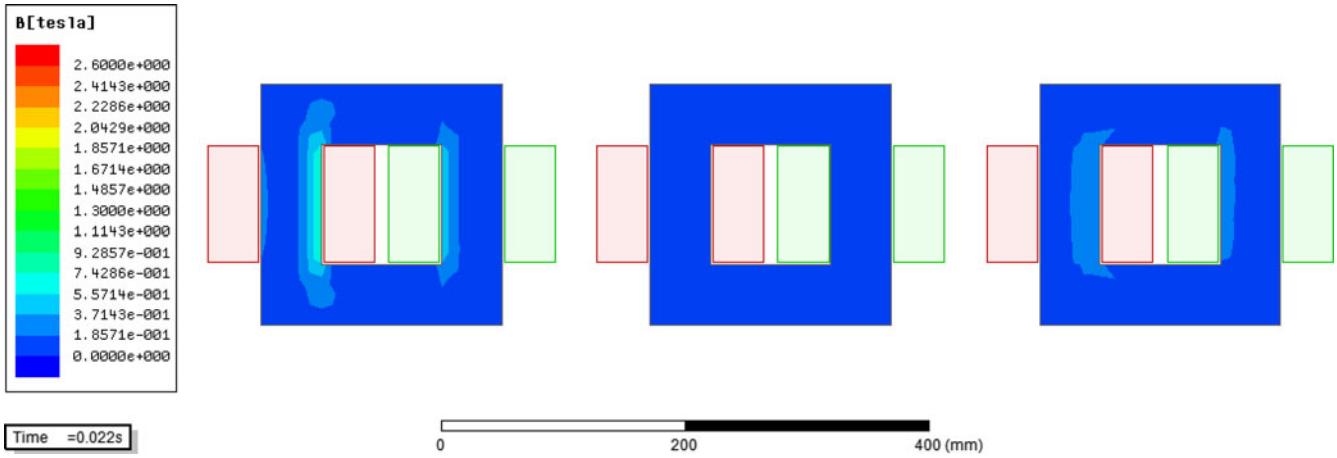


Fig. 8. Magnetic flux density in the three transformer cores during normal operations.

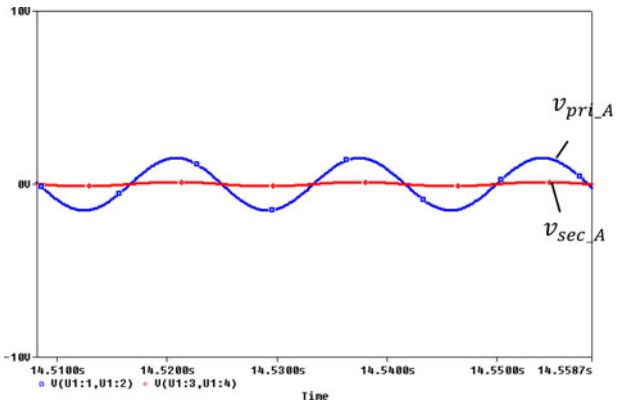


Fig. 9. Winding voltages of transformer in the NSFCL in the normal operation mode.

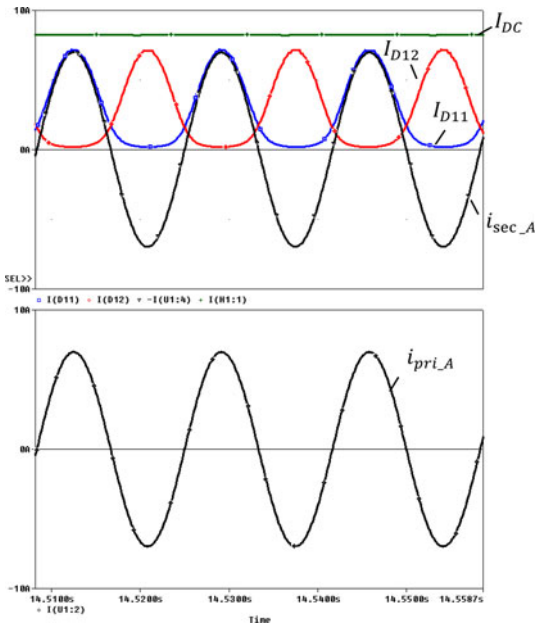


Fig. 10. Currents of the NSFCL in the normal operation mode (Upper: secondary side current; lower: primary side current).

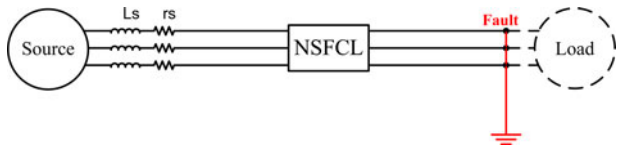


Fig. 11. Symmetrical three-phase ground fault.

mode. The cores are now heavily loaded at around the saturation point.

Fig. 13 shows the voltage waveform of the NSFCL under fault condition. When the IGBT is turned OFF, $R_d$ is presented at the terminals of the transformers' primary windings. This results in a sudden increase of the voltage across the primary windings. The voltage level is approximately the same as the system's phase-to-ground voltage (380 V in a 600 $\mathrm{V_{L-L}}$ system, as shown in Fig. 11). On the secondary side, however, the dc voltage applied to the shunt resistor $R_d$ approximately equals the magnitude of the system line-to-line voltage, which is around 850 V.

Fig. 14 shows the switching transient of the NSFCL's operation against a fault. In Fig. 14, $t_F$ is the instant when the fault occurs; $t_{\mathrm{OFF}}$ is the instant when the IGBT is being turned OFF; $t_{\mathrm{CL}}$ is the instant when the IGBT is completed OFF; $V_G$ is the gate signal of the IGBT, with high state as ON, and low state as OFF; $V_{R_d}$ is the voltage across the current limiting resistor $R_d$; $I_{\mathrm{DC}}$ is the dc branch current, which is the summation of the currents on both current paths; $I_{L_c}$ is the current flowing in the DC reactor; and $I_{D_{fw}}$ is the freewheeling diode current. At fault instant $t_F$, the rapid change of current induces a voltage in the DC reactor, which almost instantly forces a portion of the current to flow in the current limiting resistor $R_d$. The currents on both current paths ($I_{\mathrm{igbt}} = I_{L_c}$ and $I_{R_d}$) start to rise; the sum of these two currents equals the dc branch current, which is the same magnitude as the line current at the moment. After a delay, at instant $t_{\mathrm{OFF}}$, the control circuit starts to turn OFF

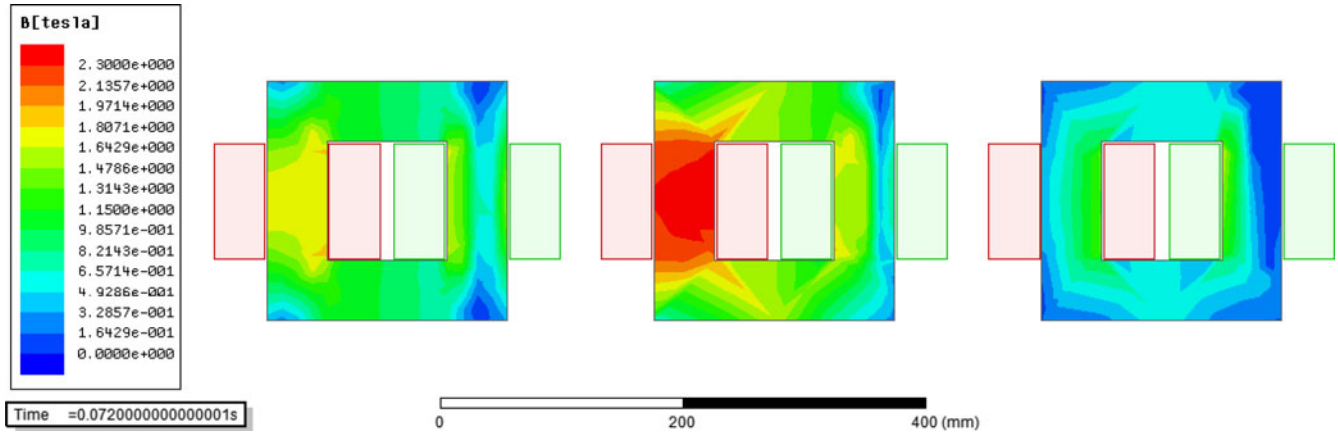


Fig. 12. Magnetic flux density in the three transformer cores during the three-phase ground fault.

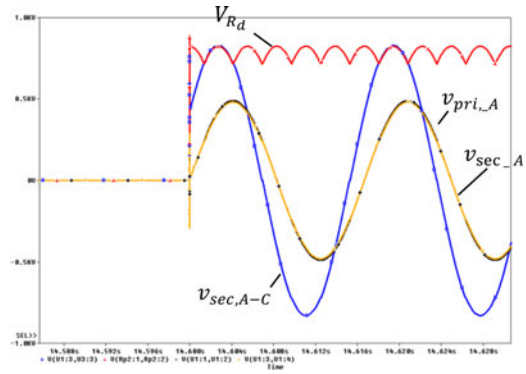


Fig. 13. Voltage waveforms of the NSFCL in the fault current limiting mode.

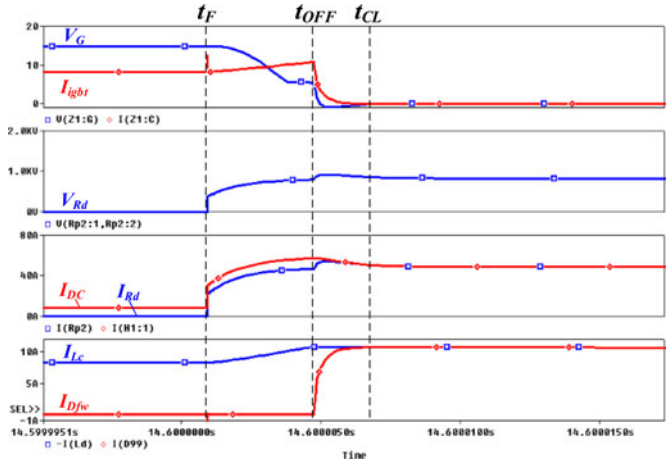


Fig. 14. Current commutation and freewheeling during fault transient.

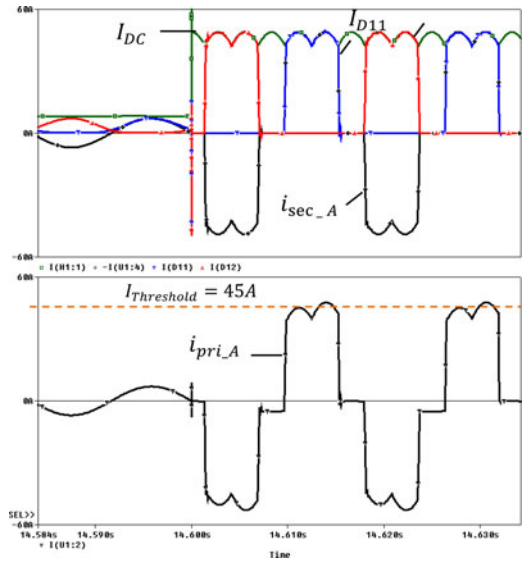


Fig. 15. Current waveforms of the NSFCL in the fault current limiting mode.

the IGBT. With the IGBT blocking the current on Current Path (i), the parallel freewheeling diode, as shown in Fig. 2, starts to discharge the energy stored in the DC reactor. At the meantime, as the current on Curent Path (i) ($I_{\rm igbt}$) drops to zero at $t_{\rm CL}$, the dc branch current $I_{\rm DC}$ becomes equal to the current on Current Path (ii) ($I_{R_d}$), meaning that the current commutation to Current Path (ii) is completed. After $t_{\rm CL}$, the current limiting resistor $R_d$ dominates the impedance in the dc branch, hence limits the fault current in the dc branch as well as on the power lines.

In Fig. 15, the ac currents on both windings of the phase A transformer are shown, along with the dc branch current. As discussed previously, during faults, the diode bridge is working in the rectifier mode with a resistive load $R_d$. Therefore, $I_{\rm DC}$ and $i_{\rm sec\_A}$ are determined by the system line-to-line voltage and the value of $R_d$, according to (9). In the simulation, the fault current is designed to be limited below $I_{\rm Threshold} = 45$ A, as shown in Fig. 15.

Note that in the benchmark system, we choose to have the NSFCL limit fault currents at $I_{\rm Threshold}$, while in a different case, the limited fault current level can be adjusted by the user by changing the resistance of $R_d$, and can be different from $I_{\rm Threshold}$.

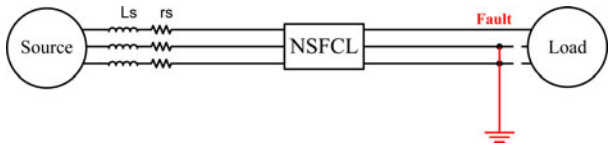


Fig. 16. Asymmetrical two-phase-to-ground fault.

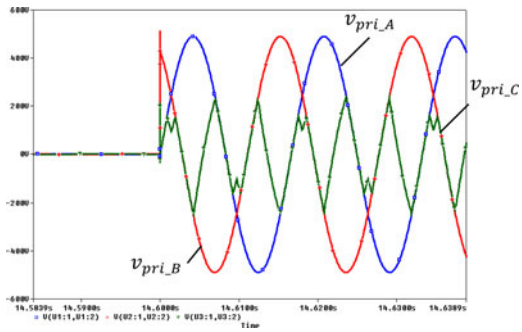


Fig. 17. Primary winding voltages of phases A and B (ground faulted) and phase C (not faulted) in asymmetrical fault condition.

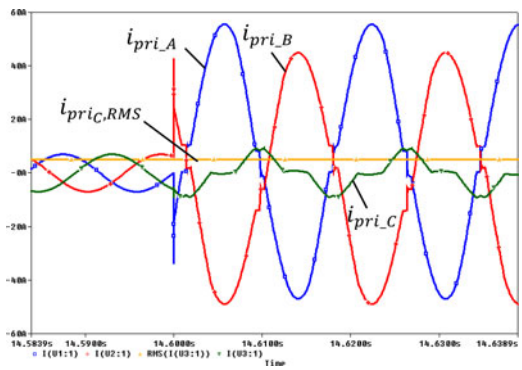


Fig. 18. AC line currents of phases A and B (ground faulted) and phase C (not faulted) in asymmetrical fault condition.

### C. Fault Current Limiting Mode (Asymmetrical Fault)

Fig. 16 describes an asymmetrical fault condition, with two phases (A and B) directly shorted to ground while phase C remains unfaulted. The voltage waveforms of the three phases' primary winding voltages are shown in Fig. 17. With $R_d$ switched in, the transformers of phases A and B are taking the full system voltage from the source. However, while not faulted, the primary winding of phase C transformer sees voltage injected from the other phases through the common point of the secondary side Y connection. This voltage has smaller amplitude, and is out of phase with phase C current.

Fig. 18 shows the waveforms of ac line currents in the two-phase ground fault condition. The peaks of the fault currents on phases A and B are limited to $I_{\mathrm{Threshold}}$, which is about the same level in a three-phase fault case. For the unfaulted phase C, the current is distorted by the induced voltage on the primary winding, as shown in Fig. 17. However, since this voltage is induced from the other phases, it only consumes the reactive power and distorts the phase C current, without affecting the RMS output to the load on phase C.

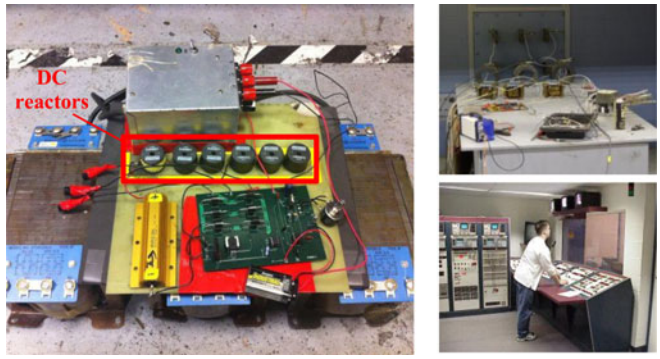


Fig. 19. NSFCL prototype and the high-power test lab.

## VII. Prototype and Experimental Results

An NSFCL prototype is designed and built for the benchmark system described in Table I. In the prototype, an external dc voltage source is used for the dc bias compensation during normal operation to demonstrate the idea. In the real product, an integrated dc–dc converter may be used to provide the bias voltage, which will not be covered in this paper. The prototype is tested in a UL-certified high-power test lab on a three-phase 600-V system. The test setup is the same as shown in Fig. 2. The balanced three-phase load is pure resistive and draws 5-A current during normal operation. A three-phase short-circuit fault is created to generate 100 kA of the potential fault current. The prototype should limit the fault current to 45 A for a short time. After 100 ms, a low-cost circuit breaker with 10-kA interrupting capacity will clear the fault. The NSFCL prototype and the UL test lab are shown in Fig. 19.

Table II compares the ratings of the prototype's components to the ratings required if the NSFCL needs to run in the fault current limiting mode in the steady state. Table II shows that by limiting the NSFCL's runtime in the fault current limiting mode to a few cycles, we are able to reduce the size, weight, and cost of these critical components that usually become bulky and expensive as their power ratings increase. For example, in prior art, the DC reactor is rated with 0.2-H inductance and with current rating of 30 A [16]. DC reactors of such ratings are usually very heavy: a 50-mH, 20-A-rated DC reactor weighs ~72 lbs [25]. While in our NSFCL prototype, the 1-mH, 6–A-rated component weighs only a few oz, as shown in Fig. 19. Also, instead of the 15-kVA transformer that is required to run the FCL in the steady state in the fault current limiting mode, our NSFCL prototype only uses 3-kVA transformers, which is ten times smaller in size and weight. Therefore, the overall size and weight of the NSFCL device can be reduced by more than ten times. Small foot print is desirable, because in many applications, space is limited. Moreover, smaller magnetic devices such as DC reactors and transformers also result in lower cost, which is another desired feature for FCLs.

TABLE II
REDUCTION IN COMPONENT RATINGS

| Type of component ratings | Ratings required to run fault condition in steady-state | Component ratings in prototype |
|---|---|---|
| Transformer power | 15 kVA | 3 kVA |
| Rectifier diode current | 45 A | 10 A |
| DC reactor coil | 45 A | 6 A |
| Current limiting resistor power | 33.5 kW | 135 W |

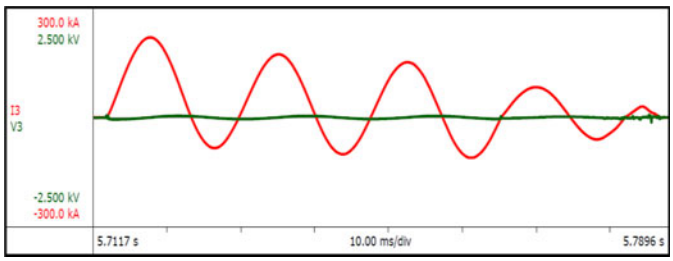


Fig. 20. Calibration waveform for the 100-kA short-circuit fault.

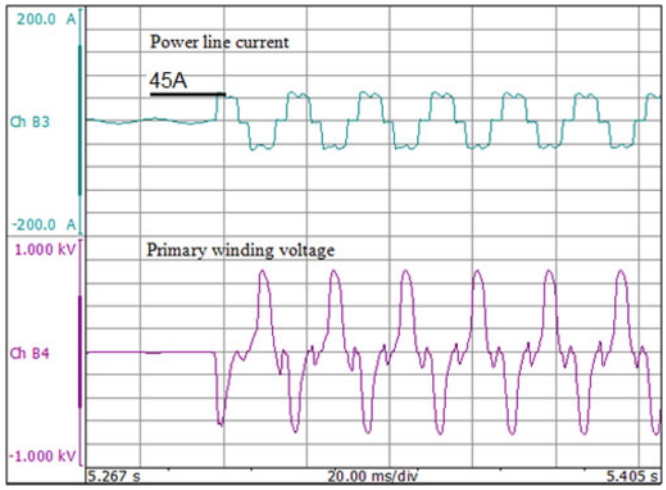


Fig. 21. Experimental results of the NSFCL operating under a three-phase short-circuit fault.

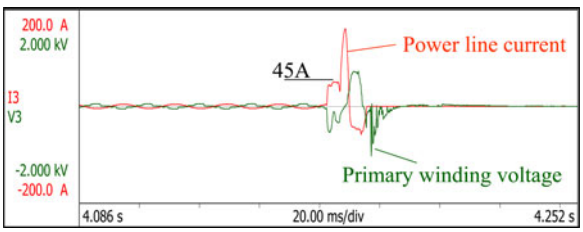


Fig. 22. Experimental results of the NSFCL operating under a two-phase short-circuit fault (faulted phase).

Fig. 20 shows the calibration waveform of the 100-kA short-circuit fault test. The maximum RMS current on the first cycle is 101.5 kA, power factor is 1.5%. With the same short-circuit fault setup, Fig. 21 shows the power line current and the primary winding voltage of phase A when a three-phase short-circuit fault is created by a remote-controlled contactor. The potential fault current is 100 kA. Almost immediately after the fault occurrence, the NSFCL prototype limits the line current at around 45-A peak. To demonstrate the operational waveforms of the NSFCL under fault conditions, we intentionally let the fault run for a few cycles without tripping by the circuit breaker.

Fig. 22 shows the current and voltage waveforms of one of the faulted phases when the NSFCL operates against an asymmetrical two-phase short-circuit fault, with potential the fault current of 100 kA. A slower circuit breaker with 10-kA interruption rating is used to interrupt the fault current after the NSFCL clamps the current long enough for the breaker to react. In this case, the potential fault current level is ten times the rated capacity of the interruption device. Without the NSFCL, the circuit breaker could be burnt by the excessive energy when it attempts to interrupt such high current. With the NSFCL, however, the fault current to be handled by the circuit breaker is only 45-A peak, although a spike of 150-A inrush current from the transformer is observed during the first half-cycle. Therefore, the 10-kA circuit breaker is able to safely trip the fault after one cycle. It should be noted that this inrush current depends on a fault phase angle as well as the transformer's characteristics; and can be minimized or eliminated with proper transformer design and building.

## VIII. CONCLUSION

In this paper, we propose an NSFCL that can limit the fault current for existing traditional protection devices with low AIR ratings. The NSFCL limits maximum fault current, eliminating the need to upgrade protective equipment. Since the switching occurs at low current levels, service life of the switching devices is extended. The fault energy level is also reduced, providing safer environment for the user and other equipment.

With simulation and experimental results, the proposed NSFCL topology is shown to be effective in limiting large fault currents for 100 ms (about six line cycles). This is a length of time sufficient for a conventional low AIR fuse or a circuit breaker to interrupt the current safely. Restricting the NSFCL's runtime in the fault current limiting mode is important. Under such condition, the NSFCL's size and weight can both be reduced by more than ten times with the topology proposed in this paper. It should be noted that, although lower cost can be expected because of the simplicity and smaller size of the NSFCL, cost comparison cannot be fairly made at this time, since most FCL topologies are still in research and development stage and are yet to be commercialized. Clearly, though, NSFCLs in general are significantly lower cost than the extremely expensive SCFCL (>$100 k). For instance, the target component price for

the proposed NSFCL is <$100. Then, there may be the additional cost of the secondary protection device, which for our application maybe a few thousand USD.

Circuit analysis for the NSFCL's normal operation mode and the fault current limitation mode with both symmetrical and asymmetrical faults are provided. Also, the paper discusses the sizing of the DC reactor and the current limiting resistor $R_d$.

To validate the concept, simulation results of a 600-V NSFCL benchmark system are presented. Additionally, experimental results of the tests of an NSFCL prototype in a UL-certified high-power lab are presented. The NSFCL successfully limits the fault current at the desired level and helps a 10-kA-rated circuit breaker to clear the fault, which has 100-kA potential fault current if the NSFCL was not used.

Nevertheless, because of the additional dc–dc converter that provides the dc bias for the bridge, the chance of device failure is increased. Moreover, since the DC reactor no longer functions as current limiting, there is a potential risk of protection failure when the IGBT is short-circuited. These are shortcomings of the NSFCL yet to be solved but will be necessary for future commercialized development.

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